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# ***XTREME* Semiconductor, LP**

## **Quality Management Program**

### **Website Copy**



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**Quality Management Plan  
Document: XP 001**

**REVISIONS**

<b>Revision</b>	<b>Description</b>	<b>Date</b>	<b>ECN</b>
-	Initial Release	05-02-2005	0001
A	Changes to Paragraph 4.0 based on DLA Land and Maritime inputs.	06-23-2005	0015
B	Changes to Paragraph 7.2.8 based on DLA Land and Maritime inputs; Added reference to XP 200 in Paragraph 3.0; updated company address; editorial changes to Paragraphs 5.1, 7.2.4, 7.4, 7.5.2, 7.8, 7.9 and 7.11.	09-16-05	0016
C	Revised paragraph 2.0 to state that XTREME Semiconductor QM Plan XP 001 shall not deviate from MIL-PRF-38535 Appendix A flow with prior DLA Land and Maritime notification and approval. Removed Note 1 from Attachment B & F as Anloy is DLA Land and Maritime approved.	01-06-06	0019
D	Updated Attachment C to reflect actual process flow and corrected the Attachments B and F to show Integra in lieu of Amkor.	01-23-06	0021
E	Updated Attachment B to add Corwil Technology as an approved vendor for assembly.	07-30-07	0026
F	Updated company address to new location in Leander TX.	01-15-09	0027
G	Updated company Logo and edited 4.0, Company Overview.	02-16-11	0028
H	Updated Attachments B and F to reflect currently approved supply partners , removed Viko and Maxwell Technologies	02-10-15	0054



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I	Corrected old reference to DSCC and DESC replacing with DLA Land and Maritime, removed non-QML activities from Attachment B, Revised para. 2.0, Scope, to more clearly define our role, revised 7.2.1 and 7.2.2 to remove reference to customer SCD, Removed non-assembly related operations from Attachment B Assembly Baseline. Added Certificate of Compliance details for each SMD Listed by XTREME Semiconductor. Updated Attachment C to agree with current approved QML product flow GAF# 1492, introduced new paragraph 7.2.4, New Technology Insertion and re-numbered subsequent paragraphs. Removed GDSI from Attachment B as an inactive supplier.	08-04-15	0055
J	Para. 3.0 removed "A" Revision from JESD625 and updated Assembly Traveler revisions, removed unused columns from Attachment B Table, Revised Attachment C "Comments" to agree with current approved assembly flow GAF1492 Rev. 6. Updated Group B Traveler to GAF 1538 to reflect current revision, Removed Solder Dip, Attachment D removed "A" suffix devices (Solder DIP) from approved list to agree with DLA Certs, revised DLA Certifications to remove Maxwell Technologies and add note about die sourced from a die bank, Attachment A added 7.2.4 New Technology Insertion to agree with Index.	12-08-15	0063
K	Revised paragraphs 7.15.1, 7.15.2 and 7.15.5 to remove spec revision of JESD625.	01-13-16	0064



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## 1.0 Purpose

The purpose of this specification and the quality procedures referenced is to detail how *XTREME* Semiconductor implements the requirements of the Quality Management Plan as defined in Appendix G of MIL-PRF-38535.

## 2.0 Scope

This procedure applies to all operations utilized by *XTREME* Semiconductor to provide QML Q level product in accordance with MIL-PRF-38535 Appendix A. Any alteration to the MIL-PRF-38535 Appendix A flow will require DLA Land and Maritime written notification and approval prior to implementation.

## 3.0 Reference Documents

MIL-PRF-38535  
MIL-STD-883  
MIL-STD-129  
JESD625  
ISO 14644-1  
ISO 14644-2  
XP 100 "Contract Review and Order Entry"  
XP 110 "Technology Review Board"  
XP 120 "Self Assessment"  
XP 130 "Vendor Selection and Assurance"  
XP 140 "Major Change Control"  
XP 160 "Corrective Action"  
XP 180 "Quality Conformance Inspection"  
XP 190 "Data Retention"  
XP 200 "Wafer/Die Qualification Process"  
XP 210 "Training"  
XP-220 "New Product qualification"

## 4.0 Company Overview

*XTREME* Semiconductor is a solutions company providing the industry with cost effective solution for mature and obsolete semiconductor products. *XTREME*

Title	Procedure	Revision	
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Semiconductor provides the high reliability market place with a reliable, long-term, and dedicated source of microelectronic products and services not available from the commercial semiconductor market place. It is a full service company offering customers the unique experience of being able to go to one source for their entire high reliability product needs ranging from industry standard through custom microcircuits. Our central goal is to assist our customers with continued product support in the Diminishing Manufacture Source (DMS) business sector, providing a reliable source for end of life products that are no longer available from original QPL/QML manufacturers. *XTREME* Semiconductor will strive to provide many of the critical services needed to support our customer's system design such as:

- **Ceramic & Hermetic Package Design & Assembly**
- **Screening to Industrial, Military, Aerospace & Customer Specified Requirements**
- **Quality Conformance Inspection**
- **Destructive Physical Analysis (DPA)**
- **Die Banking**
- **Product Sourcing hard to find DMS products**
- **Parts Management of end-of-life (EOL) procurements**

## 5.0 Mission Statement & Quality Policy

### 5.1 Mission Statement

*XTREME* Semiconductor will strive to be the “*Best in Class*” solution for customers needing a continued source of supply critical microelectronics with a commitment to provide the high reliability market place with a reliable, long-term, and dedicated source of these microelectronic products and services not available from the commercial semiconductor market place.

### 5.2 Quality Policy

*XTREME* Semiconductor shall continually develop and improve internal and external capabilities, supply chain management, services, and sourcing options that will provide “*World Class*” customer solutions in the continued supply of needed microcircuits and services.

## 6.0 Responsibilities

- 6.1 The Technical Review Board (TRB) for *XTREME* Semiconductor shall be comprised of all Senior Partners (SP) and the Quality Manager. Representative members from subcontractors and suppliers will be utilized on an ad hoc basis as dictated by the specific item under consideration.
- 6.2 The Technical Review Board (TRB) shall be responsible for maintaining and amending the QM plan as detailed in this document. It shall be responsible for implementing the Quality Management Program and associated baselines detailed herein.
- 6.3 The Quality Manager shall document the TRB deliberations and decisions. These records will be made available to the qualifying activity (QA).
- 6.4 The detailed structure and duties of the TRB is detailed in XP 110 "Technology Review Board."

## 7.0 QM Plan Outline

- 7.1 Index of certified baseline documents.
- 7.1.1 An index is detailed in Attachment A. This index maps the requirements of MIL-PRF-38535 into this document and lists supporting specifications for *XTREME* Semiconductor procedures.
- 7.2 Conversion of customer requirements.
- 7.2.1 A review of the customer's Purchase Order (PO) and any referenced specifications or additional requirements shall be reviewed by *XTREME* Semiconductor personnel prior to order acceptance. *XTREME* shall verify that it has QML certified third party subcontractors to manufacture the specific SMD(s). A review will be conducted to ensure that subcontractors have adequate capacity and material to meet the customer's quantity and schedule. This process is detailed in XP 100 "Contract Review and Order Entry."

#### 7.2.2 Device specification requirements.

The primary device specification for QML product will be the Standard Military Drawing (SMD) and the customer's PO. The PO may not reduce any requirement as specified in the SMD.

#### 7.2.3 Controlled design procedures and tools.

*XTREME* Semiconductor's intent is to provide a continued source for previously released SMD product. This SMD product will have been developed, design, qualified and released to the marketplace by prior manufacturers. Although design and development will not be a direct function of *XTREME* Semiconductor, verification will be done to assure that the product has not changed since its original design was qualified as a SMD product. This shall be done by review of the previous manufacturer's qualification data and revision levels.

#### 7.2.4 New Technology Insertion.

*XTREME* Semiconductor does not at this time envision the introduction of any new device technology under our QML Product offering. Our QML product scope is limited to re-qualification of a previously released, now obsolete SMD product specification. The SMD product we introduce as QML product will have been previously developed, designed, qualified by the original manufacturer. Should *XTREME* Semiconductor desire to introduce a new technology into our QML product offering, a detailed plan shall define the new technology, and the criteria and methodology for characterization and qualification of new technology. It shall also include the specific details of determining the potential failure mechanisms and activation energies and their respective mitigation strategies. The new technology insertion program, plan and methods shall be reviewed by the qualifying activity

#### 7.2.5 Mask generation procedures.

Mask generation procedures are not applicable to *XTREME* Semiconductor, as it does not have mask generation capabilities.



*XTREME* Semiconductor will verify that the mask set used to manufacture the product initially qualified to the specific SMD has not changed and continues to manufacture qualified product. (Reference XP 200 “Wafer/Die Qualification Process”.)

#### 7.2.6 Wafer fabrication and assembly capabilities baselined.

Assembly baselines are detailed in Attachment B. The assembly baselines are identified in a matrix showing the operation and the subcontractor (s) utilized. All operations performed will be done by DLA Land and Maritime certified QML subcontractors. Wafer fabrication baselines are not included as they are typically considered as proprietary by die manufacturers. However, *XTREME* Semiconductor shall procure die and qualify as applicable per QP 130 “Vender Selection and Assurance” and XP 200 “Wafer/Die Qualification Procedures”.

#### 7.2.7 Design, mask, fabrication, assembly and test flows.

Assembly and test flows are detailed in Attachment C. Wafer and mask fabrication are typically considered proprietary information by die manufacturers, as noted in 7.2.5. Design is not applicable as noted in 7.2.3. However, *XTREME* Semiconductor assumes full responsibility for performance of the product to all applicable specifications as defined in the specific SMD and MIL-PRF-38535.

#### 7.2.8 QML listing coverage

QML listing coverage may be found in Attachment D.

#### 7.2.9 SEC, TCV, parametric monitor (PM) programs and test procedures.

SEC & TCV must be implemented by the die design and wafer fabrication facilities during introduction of the technology to the marketplace. *XTREME* Semiconductor does not offer wafer fabrication or chip design capabilities and thus has no control over these functions.

*XTREME* Semiconductor will pursue the use of SEC, TCV, and PM's as part of evaluation of technology acquisition. If these exist, they will be utilized to their full extent. If these do not exist, *XTREME* Semiconductor will address the intent of the SEC, TCV, and PM monitors as follows:

- *XTREME* Semiconductor controls and qualifies all wafers and die for use in QML product in accordance with process specification XP200 Appendix I.
- *XTREME* monitors critical processes such as SEM, die attach, wire bond, seal, PIND, RGA, lead finish thickness, material storage (N2 flow in dry boxes, and cold storage units), temperature, humidity, and particle counts. (These process monitors are specified in the assembly and test flows contained in Attachment C.)
- Reliability and technology monitors are implemented by compliance to the Group A, B, C and D requirements of MIL-STD-883.
- Additional process monitors may be employed by subcontractors as part of their internal process control plan. *XTREME* Semiconductor reviews the individual subcontractor's process control plan for effectiveness and its ability to provide a comprehensive approach to insuring stable processes and product.

#### 7.2.10 Incoming inspection and vendor procurement.

Vendor procurement shall be of critical importance due to the *XTREME* Semiconductor's initial business model of utilizing subcontractors exclusively for all die sources, assembly, test, TCI, and associated manufacturing activities. DLA Land and Maritime QML certification shall be required of all prospective vendors as applicable. *XTREME* Semiconductor does recognize that it is responsible for its end product meeting all customer and QA requirements. Methods used for vendor selection are per specification XP 130 "Vendor Selection and Assurance" and include:

- Onsite Vendor surveys.
- Capability analysis
- Historical review of product performance
- Industry standing
- Incoming inspection requirements

#### 7.2.11 Screening and traveler.

Screening is performed to the specific quality assurance flow of Attachment C, as defined in MIL-PRF-38535, which references the screening methods of MIL-STD-883. Screening shall be documented using a traveler (or equivalent). *XTREME* Semiconductor shall ensure that the traveler used by the subcontractor contains the following characteristics as a minimum:

- Assembly, process, and screening sequences needed to comply with the specified product flow.
- Adequate provisions to identify lot formation and identification.
- Traceability of die lots and package components to the assembly lot.
- Pass/fail results of each sequence as applicable and the identification of the individual recording the results.
- Date of completion of each sequence in the flow.
- Adequate record retention requirements ensuring that the completed traveler may be retrieved for a minimum period of 5 years.
- Part marking instructions.
- Calculation and acceptance criteria of any “percent defect allowable” (PDA) imposed by device specification.

#### 7.2.12 Technology conformance inspection (TCI) procedures

The QCI requirements as detailed in Test Method 5005 of MIL-STD 883 will be used in place of the TCI requirements of MIL-PRF-38535, Appendix J (Option 1). *XTREME* Semiconductor will assure that all product shipped has completed the required QCI testing in



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accordance with paragraph A.4.5 of MIL-PRF-38535. This assurance is specified in XP 180 "Quality Conformance Inspection". If a specific subcontractor uses Option 2 in meeting TCI requirements, *XTREME* Semiconductor shall verify that DLA Land and Maritime has approved this option. A summary of Group A, B, C, and D shall be retained by *XTREME* Semiconductor that qualifies each product shipped. All QCI testing per Test Method 5005 will be summarized and reported to DLA Land and Maritime as part of the TRB status report.

#### 7.2.13 Marking.

Device marking will be per the specific requirements of the device specification and paragraph 3.6 of MIL-PRF 38535. This marking will be specified on the traveler of the subcontractor utilized.

#### 7.2.14 Rework

Rework by subcontractors is allowed only per the requirements of MIL-PRF-38535, paragraph A.3.7.1.

### 7.3 Functional organization chart

The functional organizational chart is included in Attachment E.

### 7.4 Change control program.

#### 7.4.1 Major changes

Major changes shall be defined as those listed in MIL-PRF-38535, Appendix A, Table I. Control of these changes will be managed by the TRB and the affected subcontractor per XP 140 "Major Change Control" and XP 110 "Technology Review Board". Any change that is major or affects form, fit, or function will be submitted to DLA Land and Maritime for review and approval prior to implementation.

#### 7.4.2 Required testing.

Testing required to qualify a major change shall be per the guidelines in MIL-PRF-38535, Appendix A, Table I. Deviations from these guidelines will require TRB approval along with DLA Land and Maritime concurrence.

#### 7.4.3 TRB major change responsibility.

The TRB shall manage major changes by:

- Interfacing with subcontractors to identify proposed changes.
- Review major change qualification test plan for completeness.
- Determine required customer notification.
- Manage change to insure continuity of qualified supply to customers.
- Review and approve test results.
- Appraise DLA Land and Maritime of major change status, test results, and obtain approval as appropriate.

#### 7.4.4 DLA Land and Maritime program interface.

The Quality Assurance Manager of *XTREME* Semiconductor shall be the TRB interface with DLA Land and Maritime.

#### 7.5 Failure analysis (FA).

7.5.1 *XTREME* Semiconductor will actively direct failure analysis related to any quality issue reported by a customer resulting in a product return or application problem. The Quality Manager will initiate the failure analysis and utilize independent labs and the affected subcontractor, including the die manufacture, as appropriate to determine the root cause of the failure. Corrective action will be taken to prevent reoccurrence per XP 160 "Corrective Action".

7.5.2 *XTREME* Semiconductor shall confirm as part of our Vendor Selection, that its subcontractors to have an active FA program that facilitates corrective action and continuous improvement per XP 130 "Vendor

Selection and Assurance”. Verification of the FA program shall be done during the vendor survey.

#### 7.6 Self audit program.

The Quality Manger shall coordinate a self-audit to be performed yearly on all *XTREME* Semiconductor operations per XP 120 “Self Assessment”. Compliance to the QM Plan and all supporting XP specifications will be reviewed and documented. Any discrepancies will be documented in a corrective action request (CAR). Response to CAR’s must be completed within 30 days. Follow-up verifications to evaluate the effectiveness of the corrective action will be done and documented.

#### 7.7 TRB reporting to DLA Land and Maritime.

The functions and responsibilities of the TRB are defined in XP 110 “Technical Review Board”. The items to be reported to DLA Land and Maritime are as follows:

- Current QML listings and process flows, including subcontractors.
- Reliability data from TCI testing.
- New product development plans.
- Self-audit reports.
- Field returns, FA’s and corrective actions.
- Subcontractor evaluations and changes (if any).
- TRB deliberations and decisions.

#### 7.8 Yield improvement.

As *XTREME* Semiconductor will not be directly managing a manufacturing facility, this requirement is not directly applicable. However, *XTREME* Semiconductor shall confirm as part of our Vendor Selection, that its subcontractors to have an active yield improvement program. Reference XP 130 “Vendor Selection and Assurance”.

#### 7.9 SPC Program



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As *XTREME* Semiconductor will not be directly managing a manufacturing facility, this requirement is not directly applicable. However, *XTREME* Semiconductor shall confirm as part of our Vendor Selection, that its subcontractors to have an active SPC program. Reference XP 130 "Vendor Selection and Assurance".

#### 7.10 List of test methods.

A list of test methods/conditions for suitability and subcontractors can be found in Attachment F.

#### 7.11 Calibration.

As *XTREME* Semiconductor will not be directly managing a manufacturing facility, this requirement is not directly applicable. However, *XTREME* Semiconductor shall confirm as part of our Vendor Selection, that its subcontractors to have an active calibration system. Reference XP 130 "Vendor Selection and Assurance".

#### 7.12 Retention of qualification.

*XTREME* Semiconductor will insure all components of the QM plan are maintained, updated, and implemented through its TRB system. All required screening and TCI will be verified and documented.

#### 7.13 Training

*XTREME* Semiconductor personnel will consist of professionals with experience in all phases of semiconductor manufacturing and their military/aerospace applications. Training of employees during future expansion will be trained by the staff in the specific skills as dictated by the employee job function. (Reference XP 210 "Training" for additional details.)

#### 7.14 Cleanliness and atmosphere controls.

All subcontractors utilized will be verified by *XTREME* Semiconductor as having cleanliness and atmosphere controls as DLA Land and Maritime as

described in MIL-PRF-38535, paragraph A.4.8.1.1.7. Particulate class limits shall be defined by ISO 14644-1. ISO 1466-2 may be used as a guideline for class verification.

#### 7.15 Electrostatic Discharge Sensitivity (ESD) program.

7.15.1 As *XTREME* Semiconductor will not be directly managing a manufacturing facility, this requirement is not directly applicable. However, *XTREME* Semiconductor expects its subcontractors to maintain adequate ESD control program using JESD625 as a guideline.

7.15.2 In the event that *XTREME* Semiconductor personnel handle product, ESD precautions will be taken to ensure safe handling. Product will only be handled at an ESD workstation as defined in JESD625. This station will consist of a work surface made of conductive or dissipative material. A ground wrist or heel strap will be worn to assure that the individual is grounded. As a minimum, an ESD protective (anti-static) smock will be worn.

7.15.3 Product will be package for shipment by one of the following methods:

- Unit container suitable for ESD protection.
- Conductive rails with conductive or antistatic foam plugs at both ends of the rail.
- Antistatic rail with conductive or antistatic foam plugs at both ends of the rail. Rails shall be packaged in conductive, electrostatic field shielding material.

7.15.4 Packaging of product shall be labeled with an ESD caution label and its position shall conform to the requirements of MIL-STD-129.

7.15.5 Definitions of antistatic, conductive and electrostatic field shielding shall be per JESD625.

#### 7.16 Certification and qualification test plan.



XTREME Semiconductor will typically offer product to the marketplace that has been previously qualified by QML certified manufacturers. This qualified manufacturing flow will be maintained. Any changes to this flow will be qualified prior to implementation using qualification plans based on MIL-PRF-38535 and under TRB control. Likewise, if any new products are to initially be introduced by XTREME Semiconductor, a qualification plan based on MIL-PRF-38535 will be developed by the TRB and be completed and approved prior to product release. Certification that the product has met qualification and screening requirements will be performed prior to shipment and will be documented on a Certificate of Compliance. The Certificate of Compliance will be submitted to the Qualifying Activity (DLA Land and Maritime) for approval prior to shipment.

7.17 Process for control of third party activities.

The control of third party activities will be per XP 130 “Vendor Selection and Assurance” and 7.2.9 above.

7.18 Data retention will be as specified in XP 190 “Data Retention”. Data to be retained will include the following.

- Personnel training records.
- Inspection, screening, qualification, and QCI data.
- Initial documentation and subsequent changes in design, material and processing.
- Product lot identification.
- Product traceability.
- Self-audit reports.



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## Attachment A – MIL-PRF-38535 Index Map

SECTION	TITLE	MIL-PRF-38535 REFERENCE	XTREME SEMICONDUCTOR DOCUMENT
7.1	Index of Certified Baseline Documents	G 3.3.1.a	XP 001 Attachment A
7.2	Conversion of Customer Requirements	G 3.3.1.b	XP 100
7.2.2	Device Specification Requirements	G 3.3.1.b.1	SMD
7.2.3	Controlled Design Procedures and Tools	G 3.3.1.b.2	----
7.2.4	New Technology Insertion	3.4.1.1.1	---
7.2.5	Mask Generation Procedure	G 3.3.1.b.3	----
7.2.6	Wafer Fabrication and Assembly Capabilities Baseline	G 3.3.1.b.4	XP 001 Attachment B
7.2.7	Mask, Wafer Fabrication, Assembly, and Test Flows	G 3.3.1.b.5	XP 001 Attachment C
7.2.8	QML Listing Coverage	G 3.3.1.b.6	XP 001 Attachment D
7.2.9	SEC, TCV, & Process Monitor Programs	G 3.3.1.b.7	XP 001 Attachment C
7.2.10	Incoming Inspection & Vendor Procurement Procedures	G 3.3.1.b.8	XP 130
7.2.11	Screening	G 3.3.1.b.9	XP 001 Attachment C
7.2.12	Technology Conformance Inspection (TCI) Procedures	G 3.3.1.b.10	XP 180
7.2.13	Marking	G 3.3.1.b.11	----
7.2.14	Rework	G 3.3.1.b.12	----
7.3	Functional Organization Chart	G 3.3.1.c	XP 001 Attachment E
7.4	Change Control Program	G 3.3.1.d	XP 140
7.5	Failure Analysis Program	G 3.3.1.e	XP 160
7.6	Self-Audit Program	G 3.3.1.f	XP 120
7.7	TRB Operating Procedures	G 3.3.1.g	XP 110
7.8	Yield/Quality Improvement Program	G 3.3.1.h	XP 130
7.9	SPC Program	G 3.3.1.i	XP 130
7.10	List of Test Methods for Lab Suitability	G 3.3.1.j	XP 001 Attachment F
7.11	Calibration	G 3.3.1.l	XP 130
7.12	Retention of Qualification	G 3.3.1.m	XP 110
7.13	Training	G 3.3.1.n	XP 210
7.14	Cleanliness and Atmospheric Controls	G 3.3.1.o	XP 130
7.15	Electrostatic Discharge Sensitivity (ESD) Program	G 3.3.1.p	XP 130
7.16	Certification and Qualification Test Plan	G 3.3.1.q	XP 220
7.17	Third Party Activities	G 3.3.1.r	XP 130
7.18	Data Retention	G 3.3.h	XP190



**Attachment C – Assembly and Test Flows**

<b>Operation</b>	<b>Conditions/ Method</b>	<b>Comments</b>
Material Definition & Traceability		Per Approved Traveler
Wafer/Die Lot Acceptance	XP 200	Hold for TRB on failure
Wafer Saw		
100% Die Inspection	Test Method 2010 Condition B	STOP if YIELD < 90%, QC to inform customer. Actual % YIELD
QC Inspection	Test Method 2010 Condition B	LTPD=7, SS=32, A/R=0/1
Die Attach		
Die Attach Monitor	Test Method 2019	1 sample for initial set-up ; 1 sample end of the lot) for each lot or sub-lot (CLASS B/ CLASS Q), hold for Engineering on failure
Stud Pull	Test Method 2027	1 sample for initial setup ; 1 sample end of the lot) for each lot or sub-lot (CLASS B/ CLASS Q), hold for Engineering on failure
Wire Bond		
Wire Bond Monitor	Test Method 2011	SS=15 Wires from 4 devices (min.) For each lot of sub-lot, each shift and/or every 2hrs and end of the lot. If lot was completed in < 2hrs, pull samples @ end of lot. Hold for Eng. on failure
100% Internal Visual	Test Method 2010 Condition B	STOP if YIELD < 98%, QC to inform customer. Actual % YIELD
QC Inspection	Test Method 2010 Condition B	LTPD = 5, SS=45, A/R = 0/1
Clean/Bake		
Lid Seal		
Temperature Cycling	Test Method 1010 Condition C, 10 cycles	

**Attachment C – Assembly and Test Flows (Continued)**

<b>Operation</b>	<b>Conditions/ Method</b>	<b>Comments</b>
Constant Acceleration	Test Method 2001 Condition D	
PIND Monitor	Test Method 2020 Condition A	5pcs sample per lot. Hold for engineering if there are any failures.
Marking	Per SMD	As specified on traveler.
Lead Trim		CDIP products only
Lead Trim Monitor		4 devices, first, last and two additional random samples.
Pre-burn-in Electrical	Test Method 5004 Subgroups per SMD	
Burn-in	Test Method 1015 Per SMD	
Post Burn-in Electrical	Test Method 1015 Per SMD	
PDA		5% or per SMD spec. Hold for Engineering if there are any failures.
High Temp Electrical	Test Method 5004 Subgroups per SMD	
Low Temp Electrical	Test Method 5004 Subgroups per SMD	
Group A Electrical	Test Method 5005 Subgroups per SMD	Sample = 116(0). Hold for Engineering if there are any failures.
Fine Leak	Test Method 1014 Condition A2	
Gross Leak	Test Method 1014 Condition C1	
External Visual	Test Method 2009	
Package Devices		
QC Review		



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## Attachment D – Current QML Certifications and Listings

SMD PART NUMBER	XTREME PART NUMBER	PACKAGE
5962- 8967901QC	SEI5012- TD12B	40 PIN CDIP
5962- 8967901XC	SEI5012- TE12B	44 PIN LCC
5962- 8967401QC	SEI5014- SD14B	40 PIN CDIP
5962- 8967401XC	SEI5014- SE14B	44 PIN LCC
5962- 8967402QC	SEI5014- TD14B	40 PIN CDIP
5962- 8967402XC	SEI5014- TE14B	44 PIN LCC
5962- 8967601QC	SEI5016- SE16B	44 PIN LCC
5962- 8967601XC	SEI5016- SE16B	44 PIN LCC
5962- 8967602QC	SEI5016- SD16B	40 PIN CDIP
5962- 8967602XC	SEI5016- TD16B	40 PIN CDIP
5962- 9169101QXC	SEI5101A- SD8B	28 PIN CDIP
5962- 9169101Q3C	SEI5101A- SE8B	28 PIN LCC
5962- 9169102QXC	SEI5101A- TD8B	28 PIN CDIP
5962- 9169102Q3C	SEI5101A- TE8B	28 PIN LCC
5962- 9169201QXC	SEI5102A- SDB	28 PIN CDIP
5962- 9169201Q3C	SEI5102A- SEB	28 PIN LCC
5962- 9169202QXC	SEI5102A- TDB	28 PIN CDIP
5962- 9169202Q3C	SEI5102A- TEB	28 PIN LCC



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**Attachment D – Current QML Certifications and Listings (Continued)**

FOR DEVICE CLASSES N, Q, T, or V

5962-89674  
 STANDARD MICROCIRCUIT DRAWING NUMBER

DSCC-VA Contact: Dan Wonnell  
 Telephone: 814-892-0523

DUE DATE FOR COMPLETED CERTIFICATE and/or COMMENTS

**CERTIFICATE OF COMPLIANCE**

MANUFACTURER'S NAME, LOCATION AND CAGE CODE: XTREME Semiconductor, 12908 Trails End Road, Suite E, Leander TX 78841, 3RNHD

I (We) have reviewed the enclosed drawing and hereby certify that our MIL-PRF-38535 compliant device(s), listed below meet the requirements of the SMD (The SMD Part Number includes the drawing number, rad hard designator, device type, class designator, case outline, and lead finish designator):

SMD Part Number	Vendor Part Number
5962-8967401QC	5014-SD14B
5962-8967401XC	5014-SE14B
5962-8967402QC	5014-TD14B
5962-8967402XC	5014-TE14B

(Use a C of C Continuation Sheet if more than 5 part numbers are on the SMD.)

and fabricated, assembled and tested at our plant(s) located in:

Fabrication location(s): American Microsystems, Inc., 2300 Buckskin Road, Pocatello, Idaho 83201 – Die Bank Inventory

Assembly location(s): Golden Altos, 402 South Hillview Drive, Milpitas CA 95035

Test location(s): Anloy Technologies, 1924 American Drive, Lago Vista, TX 78645

PART MEETS OR EXCEEDS THE PERFORMANCE REQUIREMENT EITHER:

as proposed, or

with essential comments as marked on draft

PART HAS COMPLETED CONVERSION OF CUSTOMER REQUIREMENTS AND IS COVERED BY CERTIFICATION AND QUALIFICATION TO MIL-PRF-38535.  YES  NO

DEVICE CLASS LEVEL  N  Q  T  V

CERTIFICATION MARK  Q/QML  QD

BURN-IN CIRCUIT IS UNDER DOCUMENT CONTROL AND AVAILABLE UPON REQUEST  YES  NO

THESE DEVICES MEET OR EXCEED THE FOLLOWING RHA ABSOLUTE MAXIMUM TEST VALUES:

BIASING TEST CIRCUIT ATTACHED (for RHA tested devices only)  YES  NO

ESD CLASS and VOLTAGE: Class 2, Tested to 2000V

I (We) understand that this certificate is not to be used nor construed as a guarantee of continued or indefinite availability as an Approved Source for the described drawing item. I further understand that this certificate does not relieve this company from conducting the required testing and lot record keeping detailed in the Standard Microcircuit Drawing. I further agree that our company will furnish a separate certificate of conformance in company format, pertaining to actual lot date codes shipped.

\_\_\_\_\_  
 Authorized Signature(s)  
 Marty Lanning, General Partner  
 Name and Title of Authorizing Official (shall be typed)

\_\_\_\_\_  
 Date  
 (858) 230-6961  
 Telephone



Company Confidential

**Attachment D – Current QML Certifications and Listings (Continued)**

FOR DEVICE CLASSES N, Q, T, or V

5962-89676  
 STANDARD MICROCIRCUIT DRAWING NUMBER

DSCC-VA Contact: Dan Wonnell  
 Telephone: 814-892-0523

DUE DATE FOR COMPLETED CERTIFICATE and/or COMMENTS

**CERTIFICATE OF COMPLIANCE**

MANUFACTURER'S NAME, LOCATION AND CAGE CODE: XTREME Semiconductor, 12908 Trails End Road, Suite E, Leander TX 78641, 3RNHD

I (We) have reviewed the enclosed drawing and hereby certify that our MIL-PRF-38535 compliant device(s), listed below meet the requirements of the SMD (The SMD Part Number includes the drawing number, rad hard designator, device type, class designator, case outline, and lead finish designator):

SMD Part Number	Vendor Part Number
5962-8967601QC	5016-SD16B
5962-8967601XC	5016-SE16B
5962-8967602QC	5016-TD16B
5962-8967602XC	5016-TE16B

(Use a C of C Continuation Sheet if more than 5 part numbers are on the SMD.)

and fabricated, assembled and tested at our plant(s) located in:

Fabrication location(s): American Microsystems, Inc., 2300 Buckskin Road, Pocatello, Idaho 83201 – Die Bank Inventory

Assembly location(s): Golden Altos, 402 South Hillview Drive, Milpitas CA 95035

Test location(s): Anloy Technologies, 1924 American Drive, Lago Vista, TX 78645

PART MEETS OR EXCEEDS THE PERFORMANCE REQUIREMENT EITHER:

as proposed, or

with essential comments as marked on draft

PART HAS COMPLETED CONVERSION OF CUSTOMER REQUIREMENTS AND IS COVERED BY CERTIFICATION AND QUALIFICATION TO MIL-PRF-38535.  YES  NO

DEVICE CLASS LEVEL  N  Q  T  V

CERTIFICATION MARK  Q/QML  QD

BURN-IN CIRCUIT IS UNDER DOCUMENT CONTROL AND AVAILABLE UPON REQUEST  YES  NO

THESE DEVICES MEET OR EXCEED THE FOLLOWING RHA ABSOLUTE MAXIMUM TEST VALUES:

BIASING TEST CIRCUIT ATTACHED (for RHA tested devices only)  YES  NO

ESD CLASS and VOLTAGE: Class 2, Tested to 2000V

I (We) understand that this certificate is not to be used nor construed as a guarantee of continued or indefinite availability as an Approved Source for the described drawing item. I further understand that this certificate does not relieve this company from conducting the required testing and lot record keeping detailed in the Standard Microcircuit Drawing. I further agree that our company will furnish a separate certificate of conformance in company format, pertaining to actual lot date codes shipped.

\_\_\_\_\_  
 Authorized Signature(s)  
 Marty Lanning, Senior Partner

\_\_\_\_\_  
 Date  
 ( 858) 230-6961

\_\_\_\_\_  
 Name and Title of Authorizing Official (shall be typed)

\_\_\_\_\_  
 Telephone





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**Attachment D – Current QML Certifications and Listings (Continued)**

FOR DEVICE CLASSES N, Q, T, or V

5962-89679

STANDARD MICROCIRCUIT DRAWING NUMBER \_\_\_\_\_ DSCC-VA Contact: Dan Wonnell  
Telephone: 614-692-0523

DUE DATE FOR COMPLETED CERTIFICATE and/or COMMENTS \_\_\_\_\_

CERTIFICATE OF COMPLIANCE

MANUFACTURER'S NAME, LOCATION AND CAGE CODE: XTREME Semiconductor, 12908 Trails End Road, Suite E, Leander TX 78641, 3RNH0

I (We) have reviewed the enclosed drawing and hereby certify that our MIL-PRF-38535 compliant device(s), listed below meet the requirements of the SMD (The SMD Part Number includes the drawing number, rad hard designator, device type, class designator, case outline, and lead finish designator):

SMD Part Number	Vendor Part Number
5962-89679D1QC	5012-TD12B
5962-89679D1XC	5012-TE12B

(Use a C of C Continuation Sheet if more than 5 part numbers are on the SMD.)

and fabricated, assembled and tested at our plant(s) located in:

Fabrication location(s): American Microsystems, Inc., 2300 Buckskin Road, Pocatello, Idaho 83201 – Die Bank Inventory

Assembly location(s): Golden Altos, 402 South Hillview Drive, Milpitas CA 95035

Test location(s): Anloy Technologies, 1924 American Drive, Lago Vista, TX 78645

PART MEETS OR EXCEEDS THE PERFORMANCE REQUIREMENT EITHER:

as proposed, or

with essential comments as marked on draft

PART HAS COMPLETED CONVERSION OF CUSTOMER REQUIREMENTS AND IS COVERED BY CERTIFICATION AND QUALIFICATION TO MIL-PRF-38535.  YES  NO

DEVICE CLASS LEVEL  N  Q  T  V

CERTIFICATION MARK  Q/QML  QD

BURN-IN CIRCUIT IS UNDER DOCUMENT CONTROL AND AVAILABLE UPON REQUEST  YES  NO

THESE DEVICES MEET OR EXCEED THE FOLLOWING RHA ABSOLUTE MAXIMUM TEST VALUES:

BIASING TEST CIRCUIT ATTACHED (for RHA tested devices only)  YES  NO

ESD CLASS and VOLTAGE: Class 2, Tested to 2000V

I (We) understand that this certificate is not to be used nor construed as a guarantee of continued or indefinite availability as an Approved Source for the described drawing item. I further understand that this certificate does not relieve this company from conducting the required testing and lot record keeping detailed in the Standard Microcircuit Drawing. I further agree that our company will furnish a separate certificate of conformance in company format, pertaining to actual lot date codes shipped.

\_\_\_\_\_  
Authorized Signature(s)  
Marty Lanning, Senior Partner  
Name and Title of Authorizing Official (shall be typed)

\_\_\_\_\_  
Date  
( 858 ) 230-6961  
Telephone



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**Attachment D – Current QML Certifications and Listings (Continued)**

FOR DEVICE CLASSES N, Q, T, or V

5962-91691  
 STANDARD MICROCIRCUIT DRAWING NUMBER

DSCC-VA Contact: Dan Wonnell  
 Telephone: 614-692-0523

DUE DATE FOR COMPLETED CERTIFICATE and/or COMMENTS

**CERTIFICATE OF COMPLIANCE**

MANUFACTURER'S NAME, LOCATION AND CAGE CODE: XTREME Semiconductor, 12908 Trails end Road, Suite E, Leander TX 78641, 3RNH0

I (We) have reviewed the enclosed drawing and hereby certify that our MIL-PRF-38535 compliant device(s), listed below meet the requirements of the SMD (The SMD Part Number includes the drawing number, rad hard designator, device type, class designator, case outline, and lead finish designator):

SMD Part Number	Vendor Part Number
5962-9169101QXC	5101A-SD8B
5962-9169101Q3C	5101A-SE8B
5962-9169102QXC	5101A-TD8B
5962-9169102Q3C	5101A-TE8B

(Use a C of C Continuation Sheet if more than 5 part numbers are on the SMD.)

and fabricated, assembled and tested at our plant(s) located in:

Fabrication location(s): American Microsystems, Inc., 2300 Buckskin Road, Pocatello, Idaho 83201 – Die Bank Inventory

Assembly location(s): Golden Altos, 402 South Hillview Drive, Milpitas CA 95035

Test location(s): Anloy Technologies, 1924 American Drive, Lago Vista, TX 78645

PART MEETS OR EXCEEDS THE PERFORMANCE REQUIREMENT EITHER:

as proposed, or

with essential comments as marked on draft

PART HAS COMPLETED CONVERSION OF CUSTOMER REQUIREMENTS AND IS COVERED BY CERTIFICATION AND QUALIFICATION TO MIL-PRF-38535.  YES  NO

DEVICE CLASS LEVEL  N  Q  T  V

CERTIFICATION MARK  Q/QML  QD

BURN-IN CIRCUIT IS UNDER DOCUMENT CONTROL AND AVAILABLE UPON REQUEST  YES  NO

THESE DEVICES MEET OR EXCEED THE FOLLOWING RHA ABSOLUTE MAXIMUM TEST VALUES:

BIASING TEST CIRCUIT ATTACHED (for RHA tested devices only)  YES  NO

ESD CLASS and VOLTAGE: Class 2, Tested to 2000V

I (We) understand that this certificate is not to be used nor construed as a guarantee of continued or indefinite availability as an Approved Source for the described drawing item. I further understand that this certificate does not relieve this company from conducting the required testing and lot record keeping detailed in the Standard Microcircuit Drawing. I further agree that our company will furnish a separate certificate of conformance in company format, pertaining to actual lot date codes shipped.

\_\_\_\_\_  
 Authorized Signature(s)  
 Marty Lanning, Senior Partner  
 Name and Title of Authorizing Official (shall be typed)

\_\_\_\_\_  
 Date  
 ( 858 ) 230-6961  
 Telephone



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**Attachment D – Current QML Certifications and Listings (Continued)**

FOR DEVICE CLASSES N, Q, T, or V

5962-91692

STANDARD MICROCIRCUIT DRAWING NUMBER \_\_\_\_\_ DSCC-VA Contact: Dan Wonnell  
Telephone: 614-892-0523

DUE DATE FOR COMPLETED CERTIFICATE and/or COMMENTS \_\_\_\_\_

**CERTIFICATE OF COMPLIANCE**

MANUFACTURER'S NAME, LOCATION AND CAGE CODE: XTREME Semiconductor, 12908 Trails End Road, Suite E, Leander TX 78641, 3RNHD

I (We) have reviewed the enclosed drawing and hereby certify that our MIL-PRF-38535 compliant device(s), listed below meet the requirements of the SMD (The SMD Part Number includes the drawing number, rad hard designator, device type, class designator, case outline, and lead finish designator):

SMD Part Number	Vendor Part Number
5962-9169201QXC	5102A-SDB
5962-9169201Q3C	5102A-SEB
5962-9169202QXC	5102A-TDB
5962-9169202Q3C	5102A-TEB

(Use a C of C Continuation Sheet if more than 5 part numbers are on the SMD.)

and fabricated, assembled and tested at our plant(s) located in:

Fabrication location(s): American Microsystems, Inc., 2300 Bucksin Road, Pocatello, Idaho 83201 – Die Bank Inventory

Assembly location(s): Golden Altos, 402 South Hillview Drive, Milpitas CA 95035

Test location(s): Anloy Technologies, 1924 American Drive, Lago Vista, TX 78645

PART MEETS OR EXCEEDS THE PERFORMANCE REQUIREMENT EITHER:

as proposed, or

with essential comments as marked on draft

PART HAS COMPLETED CONVERSION OF CUSTOMER REQUIREMENTS AND IS COVERED BY CERTIFICATION AND QUALIFICATION TO MIL-PRF-38535.  YES  NO

DEVICE CLASS LEVEL  N  Q  T  V

CERTIFICATION MARK  Q/QML  QD

BURN-IN CIRCUIT IS UNDER DOCUMENT CONTROL AND AVAILABLE UPON REQUEST  YES  NO

THESE DEVICES MEET OR EXCEED THE FOLLOWING RHA ABSOLUTE MAXIMUM TEST VALUES:

BIASING TEST CIRCUIT ATTACHED (for RHA tested devices only)  YES  NO

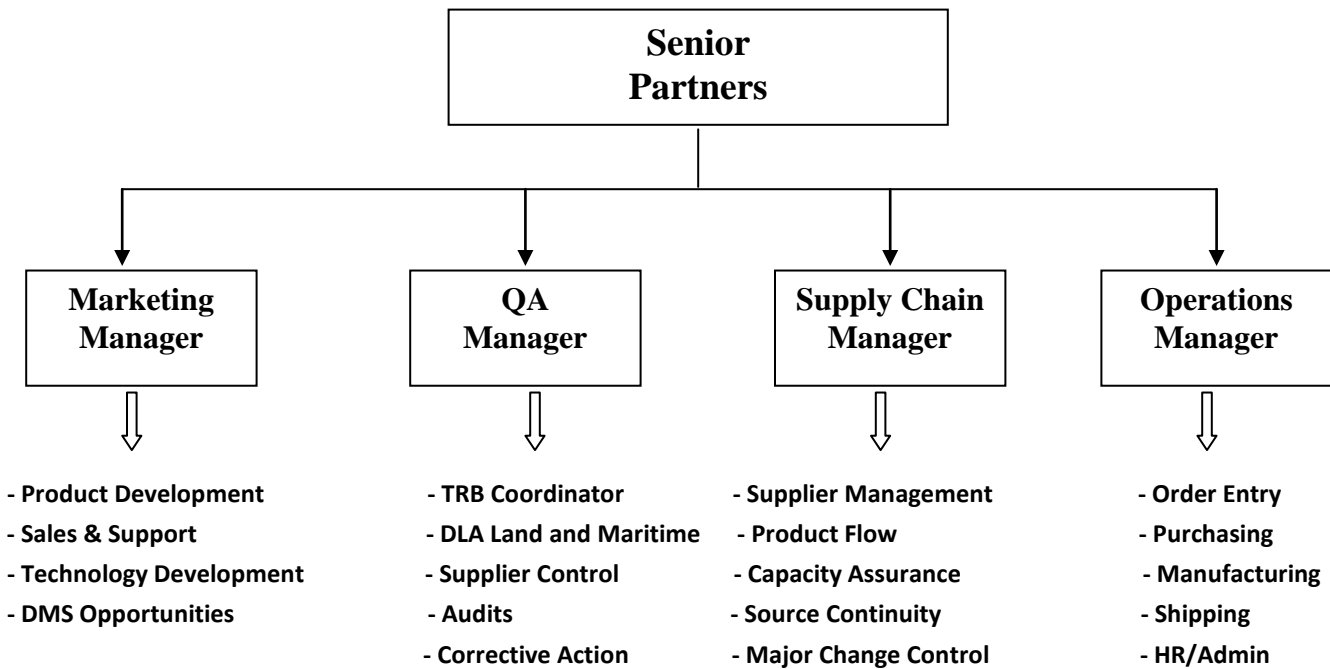
ESD CLASS and VOLTAGE: Class 2, Tested to 2000V

I (We) understand that this certificate is not to be used nor construed as a guarantee of continued or indefinite availability as an Approved Source for the described drawing item. I further understand that this certificate does not relieve this company from conducting the required testing and lot record keeping detailed in the Standard Microcircuit Drawing. I further agree that our company will furnish a separate certificate of conformance in company format, pertaining to actual lot date codes shipped.

\_\_\_\_\_  
Authorized Signature(s)  
Marty Lanning, Senior Partner  
Name and Title of Authorizing Official (shall be typed)

\_\_\_\_\_  
Date  
( 858 ) 230-6961  
Telephone

## Attachment E – Functional Organizational Chart





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## Attachment F – List of Test Methods

Test	MIL-STD 883 Method				Other
<b>Screening</b>					
Internal Visual	2010	X	X		
Temperature Cycling	1010	X	X		
Constant Acceleration	2001	X	X		
Electrical Test	SMD			X	Anloy
Burn-in	1015	X		X	Anloy
Leak Test	1014	X	X		
External Visual	2009	X	X		
<b>Group A</b>					
Electrical Test	SMD			X	Anloy
<b>Group B</b>					
Resistance to Solvents	2015	X	X		
Die Shear Test	2019/2027	X	X		
Wire Bond Pull Test	2011	X	X		
Solderability	2003	X	X		
<b>Group C</b>					
Life Test	1005			X	Anloy
<b>Group D</b>					
Physical Dimensions	2016	X			
Lead Integrity	2004	X			
Thermal Shock	1011	X			
Temperature Cycling	1010	X			
Moisture Resistance	1004	X			
Mechanical Shock	2002	X			
Vibration, Variable Frequency	2007	X			
Constant Acceleration	2001	X			
Salt Atmosphere	1009	X			
Internal Water Vapor	1018				DLA Land and Maritime Approved Labs
Adhesion of Lead Finish	2025	X			
Lid Torque	2024	X			
Resistance to solder Heat	2036	X			