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XTREME Semiconductor, LP

Quality Management Program

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For Sourcing Details

Quality Management Plan

Document: XP 001

REVISIONS

Revision	Description	Date	ECN
-	Initial Release	05-02-2005	0001
A	Changes to Paragraph 4.0 based on DSCC inputs.	06-23-2005	0015
B	Changes to Paragraph 7.2.8 based on DSCC inputs; Added reference to XP 200 in Paragraph 3.0; updated company address; editorial changes to Paragraphs 5.1, 7.2.4, 7.4, 7.5.2, 7.8, 7.9 and 7.11.	09-16-2005	0016
C	Revised paragraph 2.0 to state that XTREME Semiconductor QM Plan XP 001 shall not deviate from MIL-PRF-38535 Appendix A flow with prior DSCC notification and approval. Removed Note 1 from Attachment B & F as Anloy is DSCC approved.	01-06-06	0019
D	Updated Attachment C to reflect actual process flow and corrected the Attachments B and F to show Integra in lieu of Amkor.	01-23-06	0021
E	Updated Attachment B to add Corwil Technology as an approved vendor for assembly.	07-30-07	0026
F	Updated company address to new location in Leander TX.	01-15-09	0027

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7.16	Certification and Qualification Test Plan
7.17	Third Party Activities
7.18	Data Retention

1.0 Purpose

The purpose of this specification and the quality procedures referenced is to detail how *XTREME* Semiconductor implements the requirements of the Quality Management Plan as defined in Appendix G of MIL-PRF-38535.

2.0 Scope

This procedure applies to all operations utilized by *XTREME* Semiconductor to provide QML Q level product in accordance with MIL-PRF-38535 Appendix A to its customer base. Any alteration to the MIL-PRF-38535 Appendix A flow will require DCSS written notification and approval prior to implementation.

3.0 Reference Documents

MIL-PRF-38535
MIL-STD-883
MIL-STD-129
JESD625-A
ISO 14644-1
ISO 14644-2
XP 100 “Contract Review and Order Entry”
XP 110 “Technology Review Board”
XP 120 “Self Assessment”
XP 130 “Vendor Selection and Assurance”
XP 140 “Major Change Control”
XP 160 “Corrective Action”
XP 180 “Quality Conformance Inspection”
XP 190 “Data Retention”
XP 200 “Wafer/Die Qualification Process”
XP 210 “Training”

4.0 Company Overview

XTREME Semiconductor is a company that was founded with a commitment to provide the high reliability market place with a reliable, long-term, and dedicated source of microelectronic products and services not available from the commercial semiconductor market place. It is a full service company offering customers the unique experience of being able to go to one source for their entire high reliability product needs ranging from industry standard through custom microcircuits. Our central goal is to assist our customers with continued product support in the Diminishing Manufacture Source (DMS) business sector, providing a reliable source for end of life products that are no longer available from original QPL/QML manufacturers. *XTREME* Semiconductor will strive to provide many of the critical services needed to support our customer's system design such as:

- **Ceramic & Hermetic Package Design & Assembly**
- **Screening to Industrial, Military, Aerospace & Customer Specified Requirements**
- **Quality Conformance Inspection**
- **Destructive Physical Analysis (DPA)**
- **Die Banking**
- **Product Sourcing hard to find DMS products**
- **Parts Management of end-of-life (EOL) procurements**

5.0 Mission Statement & Quality Policy

5.1 Mission Statement

XTREME Semiconductor will strive to be the "*Best in Class*" solution for customers needing a continued source of supply critical microelectronics with a commitment to provide the high reliability market place with a reliable, long-term, and dedicated source of these microelectronic products and services not available from the commercial semiconductor market place.

5.2 Quality Policy

XTREME Semiconductor shall continually develop and improve internal and external capabilities, supply chain management, services, and sourcing options that will provide "*World Class"* customer solutions in the continued supply of needed microcircuits and services.

6.0 Responsibilities

6.1 The Technical Review Board (TRB) for *XTREME* Semiconductor shall be comprised of all Senior Partners (SP) and the Quality Manager. Representative members from subcontractors and suppliers will be utilized on an ad hoc basis as dictated by the specific item under consideration.

6.2 The Technical Review Board (TRB) shall be responsible for maintaining and amending the QM plan as detailed in this document. It shall be responsible for implementing the Quality Management Program and associated baselines detailed herein.

6.3 The Quality Manager shall document the TRB deliberations and decisions. These records will be made available to the qualifying activity (QA).

6.4 The detailed structure and duties of the TRB is detailed in XP 110 "Technology Review Board."

7.0 QM Plan Outline

7.1 Index of certified baseline documents.

7.1.1 An index is detailed in Attachment A. This index maps the requirements of MIL-PRF-38535 into this document and lists supporting specifications for *XTREME* Semiconductor procedures.

7.2 Conversion of customer requirements.

7.2.1 A review of the customer's Purchase Order (PO) and any referenced specifications or additional requirements shall be reviewed by *XTREME* Semiconductor personnel prior to order acceptance. *XTREME* shall verify that it has QML certified third party subcontractors to manufacture the specific SMD(s). Customer Source Control Drawings (SCD) will be reviewed for all applicable requirements and these requirements will be incorporated into the manufactured product. A review will be conducted to ensure that subcontractors have adequate capacity and material to meet the customer's quantity and schedule. This process is detailed in XP 100 "Contract Review and Order Entry."

7.2.2 Device specification requirements.

The primary device specification for QML product will be the Standard Military Drawing (SMD) and the customer's PO. The PO may not reduce any requirement as specified in the SMD. The device specification for SCD's will be defined in the customer's drawing.

7.2.3 Controlled design procedures and tools.

XTREME Semiconductor's intent is to provide a continued source for previously released SMD product. This SMD product will have been developed, design, qualified and released to the marketplace by prior manufacturers. Although design and development will not be a direct function of *XTREME* Semiconductor, verification will be done to assure that the product has not changed since its original design was qualified as a SMD product. This shall be done by review of the previous manufacturer's qualification data and revision levels.

7.2.4 Mask generation procedures.

Mask generation procedures are not applicable to *XTREME* Semiconductor, as it does not have mask generation capabilities. *XTREME* Semiconductor will verify that the mask set used to manufacture the product initially qualified to the specific SMD has not changed and continues to manufacture qualified product. (Reference XP 200 "Wafer/Die Qualification Process".)

7.2.5 Wafer fabrication and assembly capabilities baselined.

Assembly baselines are detailed in Attachment B. The assembly baselines are identified in a matrix showing the operation and the subcontractor (s) utilized. All operations performed will be done by DSCC certified QML subcontractors. Wafer fabrication baselines are not included as they are typically considered as proprietary by die manufacturers. However, *XTREME* Semiconductor shall procure die and qualify as applicable per QP 130 "Vender Selection and Assurance" and XP 200 "Wafer/Die Qualification Procedures".

7.2.6 Design, mask, fabrication, assembly and test flows.

Assembly and test flows are detailed in Attachment C. Wafer and mask fabrication are typically considered proprietary information by die manufacturers, as noted in 7.2.5. Design is not applicable as noted in 7.2.3. However, *XTREME* Semiconductor assumes full responsibility for performance of the product to all applicable specifications as defined in the specific SMD and MIL-PRF-38535.

7.2.7 QML listing coverage

QML listing coverage may be found in Attachment D.

7.2.8 SEC, TCV, parametric monitor (PM) programs and test procedures.

SEC & TCV must be implemented by the die design and wafer fabrication facilities during introduction of the technology to the marketplace. *XTREME* Semiconductor does not offer wafer fabrication or chip design capabilities and thus has no control over these functions.

XTREME Semiconductor will pursue the use of SEC, TCV, and PM's as part of evaluation of technology acquisition. If these exist, they will be utilized to their full extent. If these do not exist, *XTREME* Semiconductor will address the intent of the SEC, TCV, and PM monitors as follows:

- *XTREME* Semiconductor controls and qualifies all wafers and die for use in QML product in accordance with process specification XP200 Appendix I.

- *XTREME* monitors critical processes such as SEM, die attach, wire bond, seal, PIND, RGA, lead finish thickness, material storage (N2 flow in dry boxes, and cold storage units), temperature, humidity, and particle counts. (These process monitors are specified in the assembly and test flows contained in Attachment C.)

- Reliability and technology monitors are implemented by compliance to the Group A, B, C and D requirements of MIL-STD-883.

- Additional process monitors may be employed by subcontractors as part of their internal process control plan. *XTREME* Semiconductor reviews the individual subcontractor's process control plan for effectiveness and its ability to provide a comprehensive approach to insuring stable processes and product.

7.2.9 Incoming inspection and vendor procurement.

Vendor procurement shall be of critical importance due to the *XTREME* Semiconductor's initial business model of utilizing subcontractors exclusively for all die sources, assembly, test, TCI, and associated manufacturing activities. DSCC QML certification shall be required of all prospective vendors as applicable. *XTREME* Semiconductor does recognize that it is responsible for its end product meeting all customer and QA requirements. Methods used for vendor selection are per specification XP 130 "Vendor Selection and Assurance" and include:

- Onsite Vendor surveys.
- Capability analysis
- Historical review of product performance
- Industry standing
- Incoming inspection requirements

7.2.10 Screening and traveler.

Screening is performed to the specific quality assurance flow of Attachment C, as defined in MIL-PRF-38535, which references the screening methods of MIL-STD-883. Screening shall be documented using a traveler (or equivalent). *XTREME* Semiconductor shall ensure that the traveler used by the subcontractor contains the following characteristics as a minimum:

- Assembly, process, and screening sequences needed to comply with the specified product flow.
- Adequate provisions to identify lot formation and identification.
- Traceability of die lots and package components to the assembly lot.
- Pass/fail results of each sequence as applicable and the identification of the individual recording the results.

- Date of completion of each sequence in the flow.
- Adequate record retention requirements ensuring that the completed traveler may be retrieved for a minimum period of 5 years.
- Part marking instructions.
- Calculation and acceptance criteria of any "percent defect allowable" (PDA) imposed by device specification.

7.2.11 Technology conformance inspection (TCI) procedures

The QCI requirements as detailed in Test Method 5005 of MIL-STD 883 will be used in place of the TCI requirements of MIL-PRF-38535, Appendix J (Option 1). *XTREME* Semiconductor will assure that all product shipped has completed the required QCI testing in accordance with paragraph A.4.5 of MIL-PRF-38535. This assurance is specified in XP 180 "Quality Conformance Inspection". If a specific subcontractor uses Option 2 in meeting TCI requirements, *XTREME* Semiconductor shall verify that DSCC has approved this option. A summary of Group A, B, C, and D shall be retained by *XTREME* Semiconductor that qualifies each product shipped. All QCI testing per Test Method 5005 will be summarized and reported to DSCC as part of the TRB status report.

7.2.12 Marking.

Device marking will be per the specific requirements of the device specification and paragraph 3.6 of MIL-PRF 38535. This marking will be specified on the traveler of the subcontractor utilized.

7.2.13 Rework

Rework by subcontractors is allowed only per the requirements of MIL-PRF-38535, paragraph A.3.7.1.

7.3 Functional organization chart

The functional organizational chart is included in Attachment E.

7.4 Change control program.

7.4.1 Major changes

Major changes shall be defined as those listed in MIL-PRF-38535, Appendix A, Table I. Control of these changes will be managed by the TRB and the affected subcontractor per XP 140 "Major Change Control" and XP 110 "Technology Review Board". Any change that is major or affects form, fit, or function will be submitted to DSCC for review and approval prior to implementation.

7.4.2 Required testing.

Testing required to qualify a major change shall be per the guidelines in MIL-PRF-38535, Appendix A, Table I. Deviations from these guidelines will require TRB approval along with DSCC concurrence.

7.4.3 TRB major change responsibility.

The TRB shall manage major changes by:

- Interfacing with subcontractors to identify proposed changes.
- Review major change qualification test plan for completeness.
- Determine required customer notification.
- Manage change to insure continuity of qualified supply to customers.
- Review and approve test results.
- Apprise DSCC of major change status, test results, and obtain approval as appropriate.

7.4.4 DSCC program interface.

The Quality Assurance Manager of *XTREME* Semiconductor shall be the TRB interface with DSCC.

7.5 Failure analysis (FA).

7.5.1 *XTREME* Semiconductor will actively direct failure analysis related to any quality issue reported by a customer resulting in a product return or application problem. The Quality Manager will initiate the failure

analysis and utilize independent labs and the affected subcontractor, including the die manufacture, as appropriate to determine the root cause of the failure. Corrective action will be taken to prevent reoccurrence per XP 160 "Corrective Action".

7.5.2 *XTREME* Semiconductor shall confirm as part of our Vendor Selection, that its subcontractors to have an active FA program that facilitates corrective action and continuous improvement per XP 130 "Vendor Selection and Assurance". Verification of the FA program shall be done during the vendor survey.

7.6 Self audit program.

The Quality Manger shall coordinate a self-audit to be performed yearly on all *XTREME* Semiconductor operations per XP 120 "Self Assessment". Compliance to the QM Plan and all supporting XP specifications will be reviewed and documented. Any discrepancies will be documented in a corrective action request (CAR). Response to CAR's must be completed within 30 days. Follow-up verifications to evaluate the effectiveness of the corrective action will be done and documented.

7.7 TRB reporting to DSCC.

The functions and responsibilities of the TRB are defined in XP 110 "Technical Review Board". The items to be reported to DSCC are as follows:

- Current QML listings and process flows, including subcontractors.
- Reliability data from TCI testing.
- New product development plans.
- Self-audit reports.
- Field returns, FA's and corrective actions.
- Subcontractor evaluations and changes (if any).
- TRB deliberations and decisions.

7.8 Yield improvement.

As *XTREME* Semiconductor will not be directly managing a manufacturing facility, this requirement is not directly applicable. However, *XTREME* Semiconductor shall confirm as part of our Vendor Selection, that its

subcontractors to have an active yield improvement program. Reference XP 130 “Vendor Selection and Assurance”.

7.9 SPC Program

As *XTREME* Semiconductor will not be directly managing a manufacturing facility, this requirement is not directly applicable. However, *XTREME* Semiconductor shall confirm as part of our Vendor Selection, that its subcontractors to have an active SPC program. Reference XP 130 “Vendor Selection and Assurance”.

7.10 List of test methods.

A list of test methods/conditions for suitability and subcontractors can be found in Attachment F.

7.11 Calibration.

As *XTREME* Semiconductor will not be directly managing a manufacturing facility, this requirement is not directly applicable. However, *XTREME* Semiconductor shall confirm as part of our Vendor Selection, that its subcontractors to have an active calibration system. Reference XP 130 “Vendor Selection and Assurance”.

7.12 Retention of qualification.

XTREME Semiconductor will insure all components of the QM plan are maintained, updated, and implemented through its TRB system. All required screening and TCI will be verified and documented.

7.13 Training

XTREME Semiconductor personnel will consist of professionals with experience in all phases of semiconductor manufacturing and their military/aerospace applications. Training of employees during future expansion will be trained by the staff in the specific skills as dictated by the employee job function. (Reference XP 210 “Training” for additional details.)

7.14 Cleanliness and atmosphere controls.

All subcontractors utilized will be verified by *XTREME* Semiconductor as having cleanliness and atmosphere controls as described in MIL-PRF-38535, paragraph A.4.8.1.1.7. Particulate class limits shall be defined by ISO 14644-1. ISO 1466-2 may be used as a guideline for class verification.

7.15 Electrostatic Discharge Sensitivity (ESD) program.

7.15.1 As *XTREME* Semiconductor will not be directly managing a manufacturing facility, this requirement is not directly applicable. However, *XTREME* Semiconductor expects its subcontractors to maintain adequate ESD control program using JESD625-A as a guideline.

7.15.2 In the event that *XTREME* Semiconductor personnel handle product, ESD precautions will be taken to ensure safe handling. Product will only be handled at an ESD workstation as defined in JESD625-A. This station will consist of a work surface made of conductive or dissapative material. A ground wrist or heel strap will be worn to assure that the individual is grounded. As a minimum, an ESD protective (anti-static) smock will be worn.

7.15.3 Product will be package for shipment by one of the following methods:

- Unit container suitable for ESD protection.
- Conductive rails with conductive or antistatic foam plugs at both ends of the rail.
- Antistatic rail with conductive or antistatic foam plugs at both ends of the rail. Rails shall be packaged in conductive, electrostatic field shielding material.

7.15.4 Packaging of product shall be labeled with an ESD caution label and its position shall conform to the requirements of MIL-STD-129.

7.15.5 Definitions of antistatic, conductive and electrostatic field shielding shall be per JESD625-A.

7.16 Certification and qualification test plan.

XTREME Semiconductor will typically offer product to the marketplace that has been previously qualified by QML certified manufacturers. This qualified manufacturing flow will be maintained. Any changes to this flow will be qualified prior to implementation using qualification plans based on MIL-PRF-38535 and under TRB control. Likewise, if any new products are to initially be introduced by *XTREME* Semiconductor, a qualification plan based on MIL-PRF-38535 will be developed by the TRB and be completed and approved prior to product release. Certification that the product has met qualification and screening requirements will be performed prior to shipment and will be documented on a Certificate of Compliance. The Certificate of Compliance will be submitted to the Qualifying Activity (DSCC) for approval prior to shipment.

7.17 Process for control of third party activities.

The control of third party activities will be per XP 130 “Vendor Selection and Assurance” and 7.2.9 above.

7.18 Data retention will be as specified in XP 190 “Data Retention”. Data to be retained will include the following.

- Personnel training records.
- Inspection, screening, qualification, and QCI data.
- Initial documentation and subsequent changes in design, material and processing.
- Product lot identification.
- Product traceability.
- Self-audit reports.

Attachment A – MIL-PRF-38535 Index Map

SECTION	TITLE	MIL-PRF-38535 REFERENCE	*XTREME* SEMICONDUCTOR DOCUMENT
7.1	Index of Certified Baseline Documents	G 3.3.1.a	XP 001 Attachment A
7.2	Conversion of Customer Requirements	G 3.3.1.b	XP 100
7.2.2	Device Specification Requirements	G 3.3.1.b.1	SMD
7.2.3	Controlled Design Procedures and Tools	G 3.3.1.b.2	----
7.2.4	Mask Generation Procedure	G 3.3.1.b.3	----
7.2.5	Wafer Fabrication and Assembly Capabilities Baseline	G 3.3.1.b.4	XP 001 Attachment B
7.2.6	Mask, Wafer Fabrication, Assembly, and Test Flows	G 3.3.1.b.5	XP 001 Attachment C
7.2.7	QML Listing Coverage	G 3.3.1.b.6	XP 001 Attachment D
7.2.8	SEC, TCV, & Process Monitor Programs	G 3.3.1.b.7	XP 001 Attachment C
7.2.9	Incoming Inspection & Vendor Procurement Procedures	G 3.3.1.b.8	XP 130
7.2.10	Screening	G 3.3.1.b.9	XP 001 Attachment C
7.2.11	Technology Conformance Inspection (TCI) Procedures	G 3.3.1.b.10	XP 180
7.2.12	Marking	G 3.3.1.b.11	----
7.2.13	Rework	G 3.3.1.b.12	----
7.3	Functional Organization Chart	G 3.3.1.c	XP 001 Attachment E
7.4	Change Control Program	G 3.3.1.d	XP 140
7.5	Failure Analysis Program	G 3.3.1.e	XP 160
7.6	Self Audit Program	G 3.3.1.f	XP 120
7.7	TRB Operating Procedures	G 3.3.1.g	XP 110
7.8	Yield/Quality Improvement Program	G 3.3.1.h	XP 130
7.9	SPC Program	G 3.3.1.i	XP 130
7.10	List of Test Methods for Lab Suitability	G 3.3.1.j	XP 001 Attachment F
7.11	Calibration	G 3.3.1.l	XP 130
7.12	Retention of Qualification	G 3.3.1.m	XP 110
7.13	Training	G 3.3.1.n	XP 210
7.14	Cleanliness and Atmospheric Controls	G 3.3.1.o	XP 130
7.15	Electrostatic Discharge Sensitivity (ESD) Program	G 3.3.1.p	XP 130
7.16	Certification and Qualification Test Plan	G 3.3.1.q	XP 220
7.17	Third Party Activities	G 3.3.1.r	XP 130
7.18	Data Retention	G 3.3.h	XP190

Attachment B – Assembly Baselines

	Contact XTREME Semi for Details								Other
Wafer Scribe	X			X					GDSI
Substrate Cleaning	X		X	X					GDSI
Epoxy Attach and Curing	X	X	X	X					
Eutectic Solder Attach	X	X	X	X					
Die Shear Test	X	X	X	X					
Solder	X		X	X					Corfin
Al Wire Bond Manual	X	X	X	X					
AL Wire Bond Automatic	X	X	X	X					
Au Wire Bond Manual	X	X	X	X					
Au Wire Bond Automatic	X	X	X	X					
Wire Bond Pull Test	X	X	X	X					
Flip Chip Capability	X		X	X					
Optical Inspection	X	X	X	X					
Seam Seal	X	X		X					
Combo Lid Seal	X	X	X	X					
Gross Leak Test	X	X	X	X					
Fine Leak Test	X	X	X	X					
Package Marking	X	X	X	X					
Programming Devices									
Test Development		X			X	X		X	
Life Test System		X			X	X		X	
De Bug Capability		X			X	X		X	Hi-Rel Labs
PIND	X	X	X						
Centrifuge (Acceleration Testing)	X	X	X	X					
Mechanical Shock Testing	X	X	X						
Vibration Testing	X	X	X						
Burn In	X	X			X			X	
Packaging and Shipping		X					X		Falcon Electronics

Attachment C – Assembly and Test Flows

Operation	Conditions/Test Method	Process Monitors
Material Definition & Traceability		Per Approved Traveler
Wafer/Die Lot Acceptance	XP 200	Hold for TRB on failure
Wafer Saw		
100% Die Inspection	Test Method 2010 Condition B	
QC Inspection	Test Method 2010 Condition B	LTPD=10 100% rescreen on failure
Die Attach		
Die Attach Monitor	Test Method 2019	Sample=3 (0) Hold for Eng. on failure
Wire Bond		
Wire Bond Monitor	Test Method 2011	Sample=15(0) from 4 devices Hold for Eng. on failure
100% Internal Visual	Test Method 2010 Condition B	
QC Inspection	Test Method 2010 Condition B	LTPD=10 100% rescreen on failure
Clean/Bake		
Lid Seal		
Temperature Cycling	Test Method 1010 Condition C, 10 cycles	
Constant Acceleration	Test Method 2001 Condition per SMD	
PIND Monitor	Test Method 2020 Condition A	5 piece sample per lot. Hold for engineering if there are any failures.
Marking	Per SMD	As specified on traveler.

Attachment C – Assembly and Test Flows (Continued)

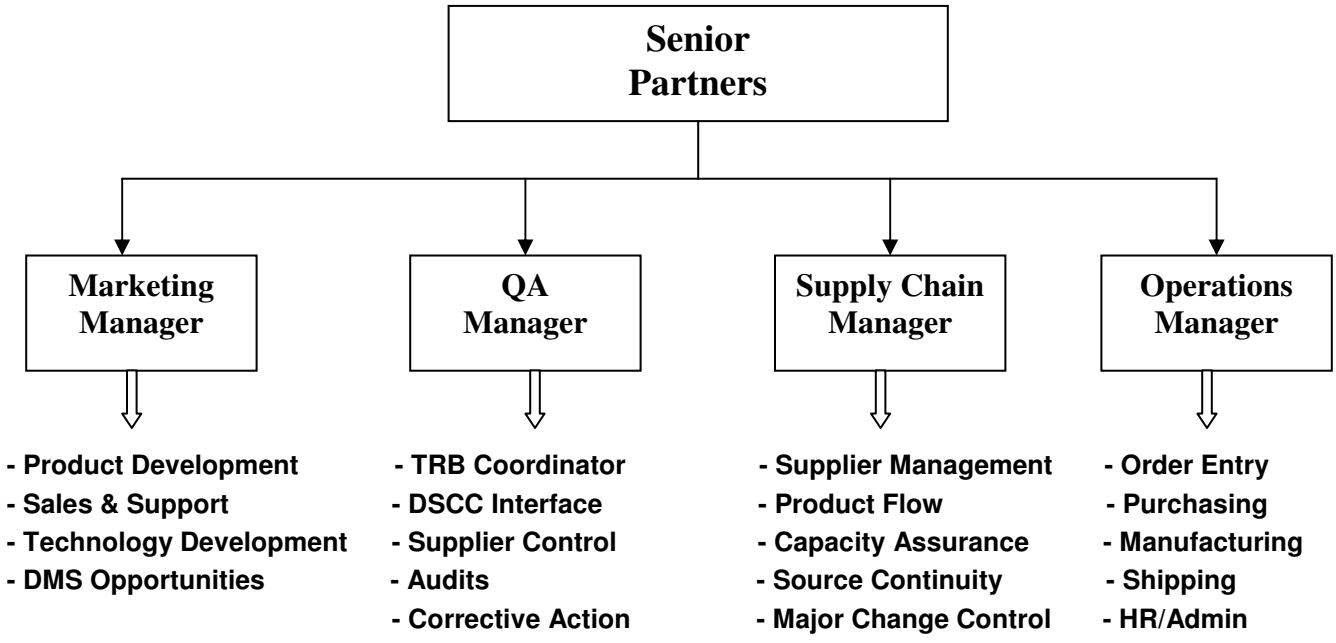
Operation	Conditions/Test Method	Comments
Lead Trim		CDIP product only.
Lead Trim Monitor		Four devices from first, last and two random samples.
Pre-burn-in Electrical	Test Method 5004 Subgroups per SMD	
Burn-in	Test Method 1015 Per SMD	
Post Burn-in Electrical	Test Method 1015 Per SMD	
PDA		5% or per SMD. Hold for Engineering if there are any failures.
High Temp Electrical	Test Method 5004 Subgroups per SMD	
Low Temp Electrical	Test Method 5004 Subgroups per SMD	
Group A Electrical	Test Method 5005 Subgroups per SMD	Sample = 116(0). Hold for Engineering if there are any failures.
Solder Dip		Lead finish "A" only
Fine Leak	Test Method 1014 Condition A1	
Gross Leak	Test Method 1014 Condition C1	
External Visual	Test Method 2009	
Package Devices		
QC Review		

Attachment D – Current QML Listings

SMD PART NUMBER	XTREME PART NUMBER	PACKAGE
5962- 8967901QC	SEI5012- TD12B	40 PIN CDIP
5962- 8967901QA	SEI5012- TD12B	40 PIN CDIP
5962- 8967901XC	SEI5012- TE12B	44 PIN LCC
5962- 8967901XA	SEI5012- TE12B	44 PIN LCC
5962- 8967401QC	SEI5014- SD14B	40 PIN CDIP
5962- 8967401QA	SEI5014- SD14B	40 PIN CDIP
5962- 8967401XC	SEI5014- SE14B	44 PIN LCC
5962- 8967401XA	SEI5014- SE14B	44 PIN LCC
5962- 8967402QC	SEI5014- TD14B	40 PIN CDIP
5962- 8967402QA	SEI5014- TD14B	40 PIN CDIP
5962- 8967402XC	SEI5014- TE14B	44 PIN LCC
5962- 8967402XA	SEI5014- TE14B	44 PIN LCC
5962- 8967601QC	SEI5016- SE16B	44 PIN LCC
5962- 8967601QA	SEI5016- SE16B	44 PIN LCC
5962- 8967601XC	SEI5016- SE16B	44 PIN LCC
5962- 8967601XA	SEI5016- SE16B	44 PIN LCC
5962- 8967602QC	SEI5016- SD16B	40 PIN CDIP
5962- 8967602QA	SEI5016- SD16B	40 PIN CDIP
5962- 8967602XC	SEI5016- TD16B	40 PIN CDIP
5962- 8967602XA	SEI5016- TE16B	44 PIN LCC
5962- 9169101QXC	SEI5101A- SD8B	28 PIN CDIP
5962- 9169101QXA	SEI5101A- SD8B	28 PIN CDIP
5962- 9169101Q3C	SEI5101A- SE8B	28 PIN LCC
5962- 9169101Q3A	SEI5101A- SE8B	28 PIN LCC
5962- 9169102QXC	SEI5101A- TD8B	28 PIN CDIP
5962- 9169102QXA	SEI5101A- TD8B	28 PIN CDIP
5962- 9169102Q3C	SEI5101A- TE8B	28 PIN LCC
5962- 9169102Q3A	SEI5101A- TE8B	28 PIN LCC
5962- 9169201QXC	SEI5102A- SDB	28 PIN CDIP
5962- 9169201QXA	SEI5102A- SDB	28 PIN CDIP
5962- 9169201Q3C	SEI5102A- SEB	28 PIN LCC
5962- 9169201Q3A	SEI5102A- SEB	28 PIN LCC
5962- 9169202QXC	SEI5102A- TDB	28 PIN CDIP
5962- 9169202QXA	SEI5102A- TDB	28 PIN CDIP
5962- 9169202Q3C	SEI5102A- TEB	28 PIN LCC
5962- 9169202Q3A	SEI5102A- TEB	28 PIN LCC

Note: Lead finish shall be specified by PO.

Attachment E – Functional Organizational Chart



Attachment F – List of Test Methods

Test	MIL-STD 883 Method	Contact XTREME Semi for Details					
Screening							
Internal Visual	2010	X	X	X			
Temperature Cycling	1010	X	X	X			
Constant Acceleration	2001	X	X	X			
Electrical Test	SMD		X		X	X	
Burn-in	1015	X	X		X	X	
Leak Test	1014	X	X	X			
External Visual	2009	X	X	X			
Group A							
Electrical Test	SMD		X		X	X	
Group B							
Resistance to Solvents	2015	X	X	X			
Die Shear Test	2019/2027	X	X	X			
Wire Bond Pull Test	2011	X	X	X			
Solderability	2003	X	X	X			
Group C							
Life Test	1005		X			X	
Group D							
Physical Dimensions	2016	X	X				
Lead Integrity	2004	X	X				
Thermal Shock	1011	X	X				
Temperature Cycling	1010	X	X				
Moisture Resistance	1004	X	X				
Mechanical Shock	2002	X	X				
Vibration, Variable Frequency	2007	X	X				
Constant Acceleration	2001	X	X				
Salt Atmosphere	1009	X	X				
Internal Water Vapor	1018						
Adhesion of Lead Finish	2025	X	X				
Lid Torque	2024	X					